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(54) FREQUENCY ADJUSTMENT CIRCUIT

(57) A circuit is provided for adjusting the average frequency of signals supplied by a frequency source, for example, in electronic time keeping devices. This circuit is preferably located between a source of clock pulses and other electronic circuitry utilizing signals from the source so that selected numbers of clock pulses may be added to or subtracted from the clock pulses being supplied to the other electronic circuitry. The circuit for adjusting the average frequency includes a first switching device connected in series with a frequency divider, a second switching device connected in parallel with at least the divider, and a control circuit for periodically opening and closing the first and second switching devices. The switching devices may be NAND-gate circuits.

FIG.1

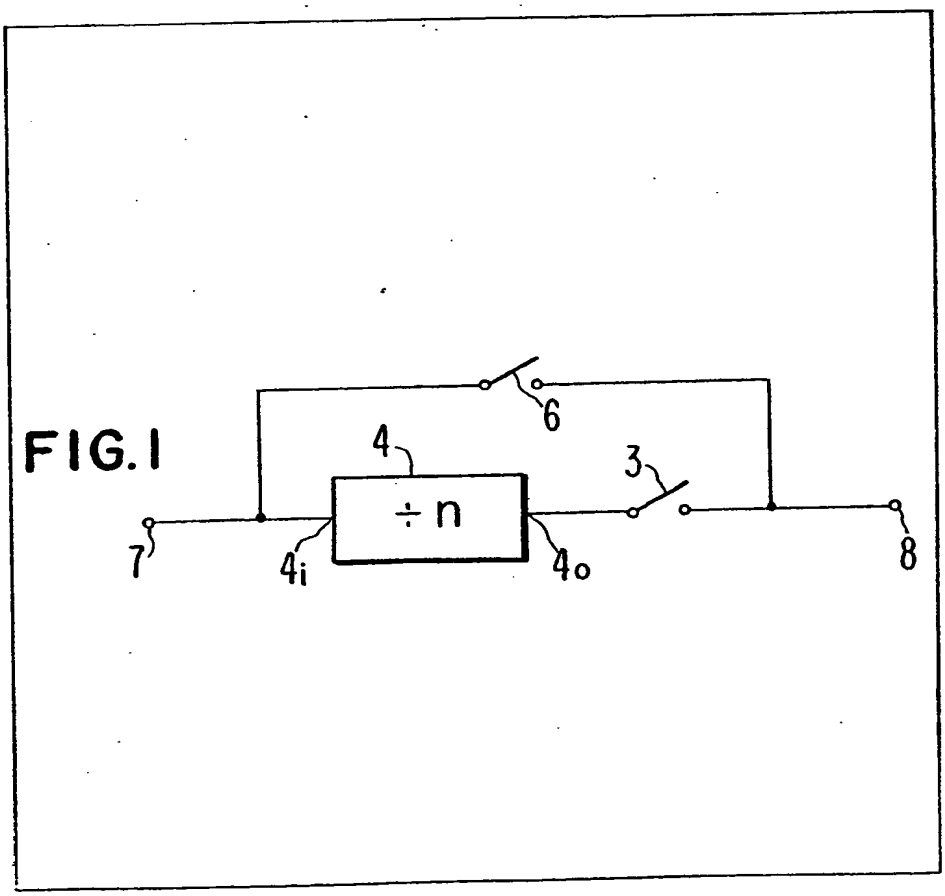


FIG.1

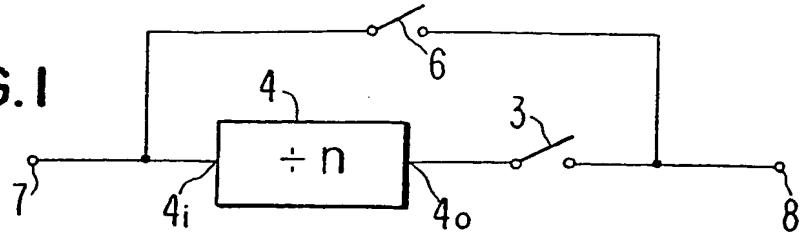


FIG.2

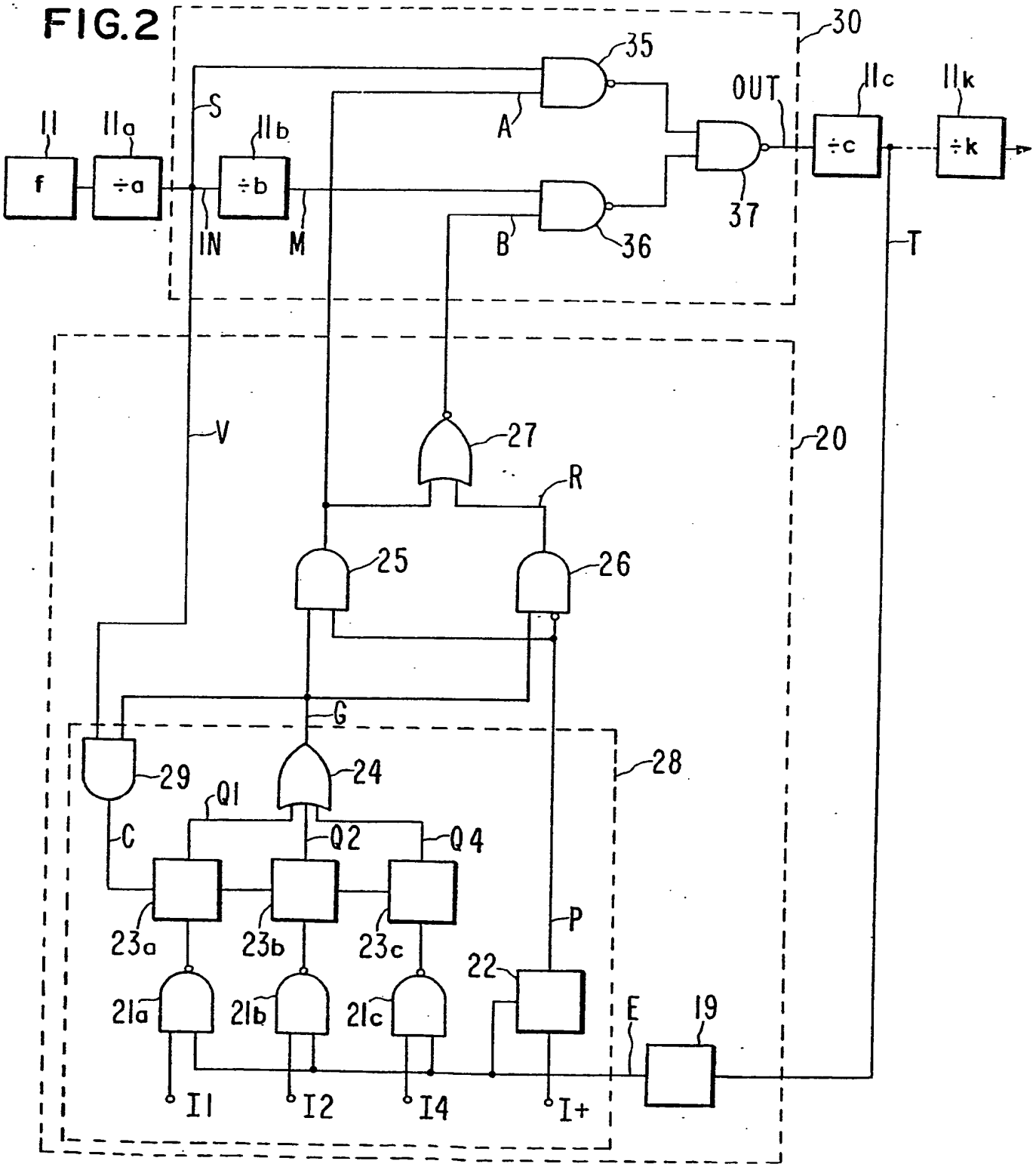
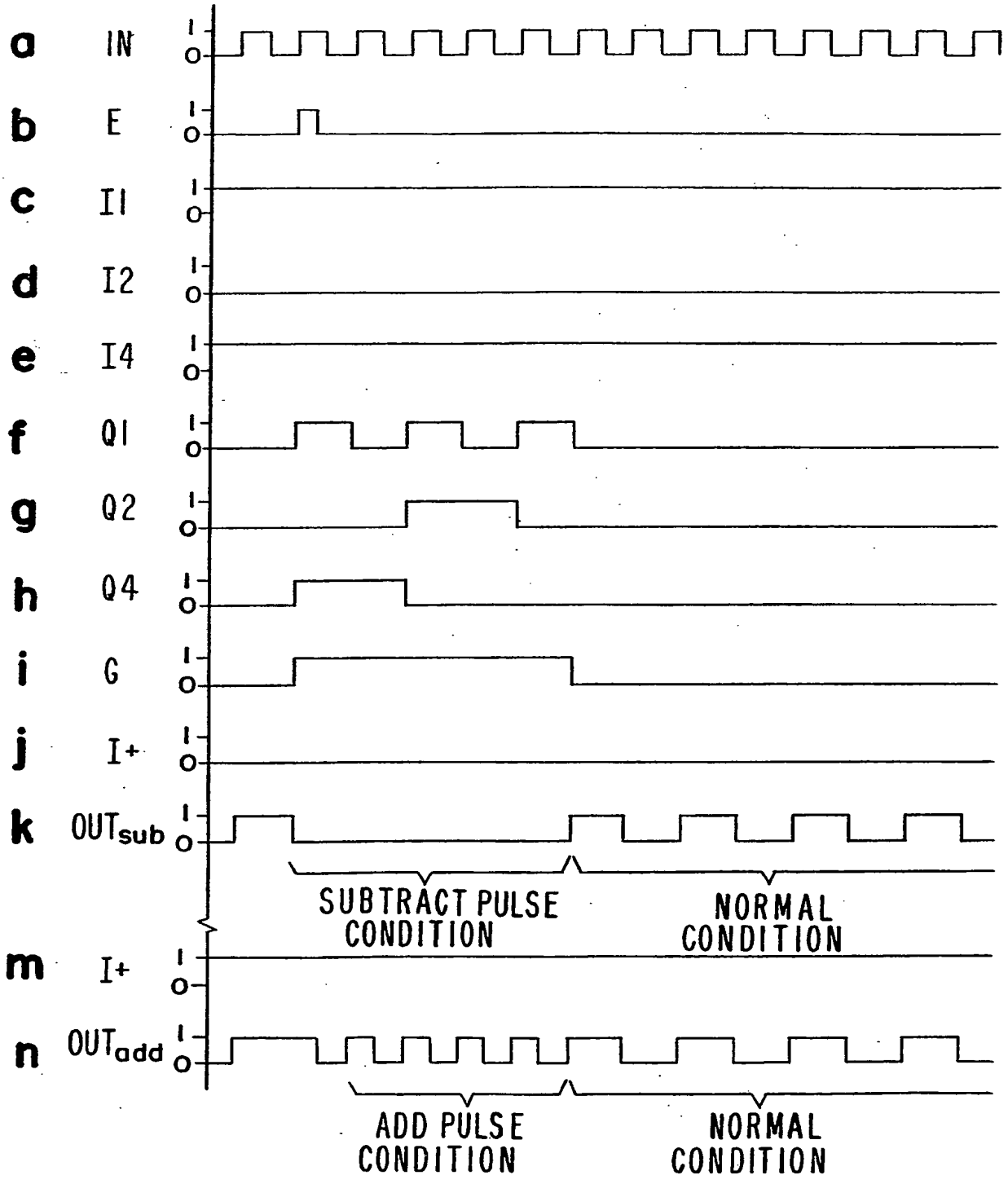


FIG.3



SPECIFICATION

FREQUENCY ADJUSTMENT CIRCUIT

This invention relates to electronic digital circuits, and in particular, to a method and apparatus for adjusting the average frequency of pulses being supplied to an electronic circuit.

Digital circuits which supply periodic electronic pulse signals to other electronic circuits are well known in the digital circuit arts and have been used in numerous devices, for example, electronic timekeeping apparatus. In typical prior art devices, a stable high frequency oscillator, typically a quartz crystal, is used to control the frequency of pulses or electronic signals supplied to other circuitry which utilizes the pulses for time keeping, counting or various other uses. Because the resonant frequency of quartz crystals differs from one to another, a pair of capacitors are typically employed with the quartz crystal or oscillator to further adjust and stabilize the frequency of oscillation. Typically, one of these capacitors is fixed, while the other is variable. During assembly of the particular circuit or product utilizing the frequency source, the variable capacitor is adjusted to cause the oscillator to generate the precise frequency of oscillation desired. Unfortunately, this adjustment is time consuming, and the variable capacitor involved is bulky and expensive. These disadvantages are particularly limiting with regard to electronic wrist watches because the quartz crystal frequency source, and all associated components, must be packaged in a sufficiently small and lightweight container to be worn on the wrist.

The importance of precise adjustment of the frequency being supplied by a frequency source may be readily understood with reference to the electronic time keeping arts. In prior-art watches or other electronic time keeping devices, a stable high frequency oscillator usually supplies signals to a series of frequency dividers or counters which progressively reduce the frequency of the signals to a desired value, for example, 1 hertz. The 1 hertz signal then may be used to drive a series of counters with a first scale of 60 counter providing a count representative of the correct number of seconds elapsed in a given minute, and a second scale of 60 counter driven by the first counter providing a count representative of the correct minute of the hour. A scale of 12 counter driven by the minutes counter will provide a count representative of the correct hour of the day, and if desired, additional counters may be provided to count days of the week, days of the month, months of the year, leap years, etc. Typically the outputs of each of the time keeping counters are decoded and coupled to a display, for example, a liquid crystal or light emitting diode display. The resulting visual output provides an indication of the time. One example of a prior-art electronic watch utilizing a series of frequency dividers or counters is U.S. Patent No. 3,815,354 issued to Sirocka et al.

Because of the extreme accuracy of the high frequency signal provided by the quartz crystal and associated circuitry, electronic time keeping devices which utilize this type of circuitry are substantially more accurate than conventional mechanical clock and watch movements. Further, the fully electronic systems are simpler to manufacture, have a much longer lifetime, and are usually of lower cost.

One example of a circuit which allows periodic adjustment of the frequency of a quartz crystal oscillator is disclosed in Swiss patent application 3863/73, published for opposition. The circuit disclosed therein utilizes a switch to selectively engage and disengage capacitors to effect the oscillation of the quartz crystal.

SUMMARY OF THE INVENTION

Applicants have discovered a highly accurate means for adjusting the average frequency of oscillation of a signal being used to drive other circuitry. The term "average frequency" is used herein in its ordinary sense, that is, to refer to the arithmetical mean frequency supplied by a circuit during a selected time period. The average frequency of a signal over a selected period is calculated by summing the products of the various instantaneous frequencies with their respective durations and dividing by the sum of the respective durations. For example, if frequency f_1 lasts for period t_1, frequency f_2 for t_2, and frequency f_3 for t_3, then the average frequency $f_{average}$ is given by:

$$f_{average} = \frac{f_1 t_1 + f_2 t_2 + f_3 t_3}{t_1 + t_2 + t_3}$$

Obviously the average frequency will not necessarily, or even usually, be equal to any of the instantaneous frequencies.

Applicants' invention, although useful in any application where a precise average frequency must be supplied, is particularly suitable for application to electronic time keeping. In such embodiments, the circuit which applicants have discovered will be situated between a frequency source and other electronic circuitry utilizing signals from the frequency source. Applicants' invention may be used with particular advantage if the other electronic circuitry utilizes signals of significantly lower frequency than those generated by the frequency source.

Applicants' circuit for adjusting the average frequency of signals supplies to another circuit includes a first switch means connected in series with a frequency dividing means and a second switch means connected in parallel with at least the dividing means. Control means are provided for selectively engaging and disengaging for desired periods of time the first and second switch means. In one preferred embodiment, the second switch means is connected in parallel with both the first switch means and the dividing means.

When applicants' circuit is in the state in which pulses are neither being added to nor subtracted from the signal being supplied by the frequency

generating means, the first switch means will be closed and the second switch means will be open. This position of the first and second switch means allows electronic signals from the frequency generating means to pass through the dividing means and be supplied to whatever other electronic circuit is desired. The frequency of the signals being supplied to the other electronic circuit will be related to the frequency of the signals generated by the generating means only by the effect of the dividing means. This condition of applicants' circuit is referred to herein as the normal condition.

When the average frequency of signals supplied to the other electronic circuitry is to be increased, the first switch means will be opened and the second switch means will be closed for a selected period of time. This switch condition is referred to herein as the "add pulse" condition. In this manner signals will pass from the frequency generating means to the other electronic circuitry without passing through the dividing means. Such signals will therefore be at a higher frequency than the previous "normal" signals which passed through the dividing means. By controlling the duration of the add pulse condition and by shifting back and forth between this condition and the normal condition the average frequency supplied to the other electronic circuitry can be increased to any desired frequency between the normal frequency and the frequency supplied by the frequency generating means. By appropriate pulsing of applicants' circuit from the normal condition into the add pulse condition, the average frequency of the signals supplied to the other electronic circuitry can be maintained at an increased frequency above the normal frequency for any desired period of time. For example, if it is desired that the average frequency supplied to the other electronic circuitry is to be higher over relatively long periods of time, then applicants' circuitry can be slowly alternated between the normal and the add pulse condition. On the other hand, if the desired higher average frequency is to exist over shorter periods of time, then the add pulse condition of applicants' circuitry will be achieved more frequently but for shorter periods.

If it is desired to reduce the average frequency of the signals from applicants' circuit, both the first and second switching means may be opened periodically. During any interval in which both the first and second switch means are open, no signal will be supplied to the other circuit, and consequently the average frequency, over some longer period of time, will be less than that normally supplied.

In one embodiment particularly suited for application to the electronic timekeeping arts, the invention will be utilized to adjust the average frequency supplied by a circuit containing a frequency source. The capability of adjusting a frequency, for example, supplied by a quartz crystal, is advantageous as it facilitates the use of lower cost quartz crystals having a wider deviation of actual frequency from that nominally desired.

The invention is further advantageous over prior-art circuits because the adjustment of the average frequency is accomplished in a linear manner, that is, a linear relationship exists between the number of counts added or subtracted and the resulting change in the average frequency. The frequency of signals supplied by the frequency-generating means can be suitably adjusted to match the desired characteristics of the remainder of the electronic circuitry. Thus, the oscillator circuit may be standardized and small electronic adjustments made to the average frequency rather than adjusting the instantaneous frequency of the source.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic diagram representing the principle of operation of applicants' invention.

Figure 2 is a logic diagram of one embodiment of applicants' invention.

Figure 3 is a timing diagram of the circuit shown in Figure 2.

DETAILED DESCRIPTION

A schematic diagram generally illustrating the principle of operation of one embodiment of the invention is shown in Figure 1. A first switching means 3 is connected in series with a frequency divider 4. Frequency divider 4 will divide the frequency supplied to its input 4i to a lower frequency which will appear at its output 4o. Frequency dividers such as frequency divider 4 are well known in the art and are commercially available, typically dividing the input frequency by an integer. An example of such a frequency divider is Fairchild Camera and Instrument Corporation (hereinafter Fairchild) product 34518. In one embodiment, second switching means 6 is connected in parallel with first switching means 3 and frequency divider 4. In operation, a frequency is supplied to terminal 7 as shown in Figure 1. By selectively opening and closing first switching means 3 and second switching means 6 for desired periods of time, a higher or lower average frequency (relative to that frequency normally supplied by divider 4 at output terminal 4o) will appear at terminal 8. The time-averaged frequency appearing at terminal 8 may be as high as that supplied to terminal 7, or as low as zero. If no change in the frequency is desired, first switching means 3 will be closed and second switching means 6 will be opened to allow the signals supplied to terminal 7 to pass through divider 4 and appear at terminal 8. This condition is referred to as the normal condition because the frequency supplied is changed only the the effect of divider 4.

As shown in Figure 1, by opening first switching means 3 and closing second switching means 6 the signals appearing at terminal 7 bypass divider 4 and appear directly at terminal 8. This condition of the circuit is referred to herein as the "add pulse" condition. This add pulse condition may be maintained for any desired period of time, thereby adjusting the average frequency appearing at terminal 8 upward. For example, if, during a given

time period, the add pulse switch condition is maintained for one-half of the period, then the average frequency of the signal appearing at terminal 8 will be mid-way between the frequency supplied at terminal 7 and the frequency normally supplied at terminal 8 (with first switching means 3 closed and second switching means 6 opened). In general, for the circuit shown in Figure 1, the average frequency (f_{ave}) supplied to terminal 8 will be related to the input frequency f_{in} supplied to terminal 7 as follows:

$$f_{ave} = \frac{f_{in}(T-t) \pm nf_{in}t}{nT}$$

where T is the time between adjustment periods to the average frequency, t is the duration of the adjustment, and n is the number (divisor) by which dividing circuit 4 divides f_{in}. Thus, if the frequency appearing at terminal 8 is to be 10 per cent higher than the normal frequency appearing at terminal 8, and n = 2, then the add pulse switch condition of the circuit will be maintained for 10 percent of the total operating time. By more rapidly switching the circuit shown in Figure 1 between the normal condition and the add pulse condition, the instantaneous frequency appearing at terminal 8 will more closely approach the desired average frequency over progressively shorter time periods.

In a similar manner the circuit shown in Figure 1 may be operated to cause the average frequency appearing at terminal 8 to be less than that normally supplied. This condition is referred to herein as the subtract pulse conditon and is achieved by opening both the first switching means 3 and the second switching means 6. When both the first switching means 3 and the second switching means 6 are open for a selected time, no pulses will be transmitted from terminal 7 to terminal 8. Thus, over some longer time period the average frequency appearing at terminal 8 will be reduced. For example, if n = 2, and if the average frequency at terminal 8 is to be 10 percent less than the normal frequency, then switch 3 and switch 6 together will be open 10 percent of the time. This condition is achieved by holding switch 6 open and then opening switch 3 10 percent of the time.

Figure 2 shows a logic diagram of one embodiment of the circuit of applicants' invention together with associated external circuitry 11, 11a, 11b...11_k, as typically is utilized in the electronic time keeping arts. Applicants' circuit includes a switching circuit 30 and a control circuit 20. Shown in Figure 2 are a frequency generator 11, a series of frequency dividers 11a, 11b...11_k. Applicants' circuit as shown in the logic diagram enclosed within dashed line blocks 20 and 30 is connected between frequency dividers 11a and 11b on the left hand side of Figure 2 and by line T between frequency dividers 11c and 11_k on the right hand side of Figure 2. It should be understood that these locations are for illustrative purposes only and that any desired location may be selected, depending upon the normal frequency desired, the extent of the maximum expected adjustment to the normal frequency, and the minimum time period during which the average new frequency is desired. For example, if the adjustment to the input frequency is desired to be made less frequently, then line T may be connected between dividers further from divider 11c, for example, following divider 11f (not shown) so monostable multivibrator 19 is triggered less frequently.

The logic diagram shown in Figure 2 includes switching circuit 30 and control circuit 20. Switching circuit 30 accomplishes the same function as the circuit shown in Figure 1. Frequency divider 11b in Figure 2 performs the function of frequency divider means 3 in Figure 1, the combination of NAND gates 36 and 37 in Figure 2 performs the function of first switching means 3 in Figure 1, and the combination of NAND gates 35 and 37 in Figure 2 performs the function of second switching means 6 in Figure 1. Thus by appropriate control of NAND gates 35, 36 and 37 the average frequency supplied to divider 11_k can be adjusted to any desired frequency between zero and the frequency of the signals presented to divider 11b on line IN.

The control circuit shown inside dashed line 20 serves to enable and disable NAND gates 35 and 36, and therefore NAND gate 37, at appropriate intervals to result in the desired average frequency being supplied to divider 11_k.

If the desired average frequency of signals on line OUT is sought to be equal to the normal frequency (the frequency on line M after division by divider 11b) then NAND gate 36 will be enabled and NAND gate 35 disabled. This is accomplished by presenting a logical 1 on line B and a logical 0 on line A. In this condition NAND gate 36 is enabled, NAND gate 35 is disabled, and NAND gate 37 is enabled. Thus signals supplied on line IN pass through divider 11b and are supplied to line OUT. This condition corresponds to the condition shown in Figure 1 if switch 6 is open and switch 3 is closed (normal operation).

If the circuit of Figure 2 is to supply an average frequency higher than the normal frequency, then NAND gate 35 will be enabled and NAND gate 36 disabled by presenting a logical 1 on line A and a logical 0 on line B. Signals supplied to circuit 30 on line IN thereby travel on line S, bypass divider 11b, and pass through NAND gates 35 and 37 to appear on line OUT. Therefore, the signals appearing on line OUT, for the period during which NAND gate 35 is enabled and NAND gate 36 disabled, will be equal in frequency to those on line IN.

If the circuit is to supply an average frequency lower than the normal frequency, both NAND gate 35 and NAND gate 36 will be disabled to prevent the transfer of any signals from line IN to line OUT. This subtract pulse condition is achieved by presenting a logical 0 on line A and a logical 0 on line B to disable both NAND gates 35 and 36. During some longer time period the average frequency of signals presented on line

OUT will be less than the normal frequency.

The control circuitry included within dashed block 20 can be any circuit which achieves the results discussed above. That is, the control circuit must properly open and close the gates 36, 37 and 38 by presenting a logical 0 to both lines A and B during a subtract pulse condition, a logical 1 to line A and a logical 0 to line B during an add pulse condition, and a logical 0 to line A and a logical 1 to line B during a normal condition. A preferred embodiment of a logic circuit which performs these functions is shown within block 20 of Figure 2. Those skilled in the digital circuit arts will realize that numerous other control circuits in addition to the one shown in Figure 2 will accomplish the desired result. One group of such circuits may be achieved using deMorgan's Theorem. In particular, for the particular embodiment of the switching circuit shown, any control circuit will be suitable which satisfies the following conditions:

A = 1 When both G = 1 and P = 1
B = 0 When either,
1) G = 1 and P = 0, or
2) A = 1

The logic diagram within block 20 of Figure 2 includes means for appropriately pulsing lines A and B to control the condition of switching circuit 30 and includes, within block 28, means for controlling the number of pulses added or subtracted.

The signal supplied to line G by the circuit within block 28, together with the signal on line P supplied by latch 22 will determine the condition of lines A and B. As will be explained, the existence and duration of a logical 1 signal on line G is used to control the existence and duration of both the add pulse and subtract pulse signal being supplied to lines A and B. If the switching circuit within block 30 is to be in its normal position, then a logical 0 will be presented to line G by the circuit within block 28. Assume, however, that a logical 1 is presented to line G by the circuit within block 28. A logical 1 on line G will enable AND gate 25 and AND gate 26. The choice of whether line A or line B is presented with a logical 1 will therefore be determined by the condition of line P. Latch 22, well known in the art, for example, Fairchild product 34042, is preset so that the presence of a logical 1 at terminal I+ will latch line P to a logical 1 state. The logical 1 on line P is inverted by the inverter preceding AND gate 26 to a logical 0, and consequently, AND gate 26 is not enabled, resulting in a logical 0 appearing on line R. The logical 1 on line P, however, in conjunction with the logical 1 on line G, causes AND gate 25 to supply a logical 1 to line A. The logical 1 on line A with the logical 0 on line R causes NOR gate 27 to supply a logical 0 at line B thereby disabling NAND gate 36. The enabling of NAND gate 35 and the disabling of NAND gate 36 places switching circuit 30 in an add pulse condition—to bypass divider 11b.

Switching circuit 30 is placed in a subtract pulse condition by supplying a logical 0 to input terminal I+ at the same time a logical 1 is presented on line G. The logical 0 at terminal I+ causes a logical 0 to appear on line P thereby disabling NAND gate 25 which disables NAND gate 35. The logical 0 on line P together with the assumed logical 1 on line G enables AND gate 26 and causes a logical 1 to appear on line R. The logical 1 on line R together with the logical 0 on line A cause NOR gate 27 to apply a logical 0 to line B. The combined logical 0's on line A and line B disable NAND gate 35 and NAND gate 36, also disabling NAND gate 37. During the period NAND gate 37 is disabled no signal appears on line OUT.

The normal condition of switching circuit 30 occurs whenever circuit 28 applies a logical 0 to line G. The logical 0 on line G disables AND gate 25 and AND gate 26 causing logical 0's to appear on line R and line A. These logical 0's disable NAND gate 35 and cause NOR gate 27 to apply a logical 1 to line B thereby enabling NAND gate 36. The logical 1 presented on line B of NAND gate 36 allows the signals on line M from divider 11b to pass through NAND gate 36 and NAND gate 37 thereby appearing in line OUT.

Thus the presence of a logical 1 at input terminal I+ together with logical 1 on line G causes switching circuit 30 to bypas divider 11b and effectively increase the average frequency of signals present on line OUT. The presence of a logical 0 at terminal I+ and a logical 1 on line G causes switching circuit 30 to interrupt the flow of signals between line IN and line OUT, thereby lowering the average frequency. Finally, the presence of a logical 0 on line G allows the signals to pass through divider 11b and appear directly on line OUT.

The purpose of the circuit within block 28 is to control the number of pulses added or subtracted by the switching circuit 30. As has been previously explained whether pulses are added or subtracted is controlled by the presence of a logical 1 or a logical 0, respectively, on line P. Addition or subtraction of pulses occurs whenever a logical 1 is presented on line E, thereby enabling NAND gates 21a, 21b, and 21c. The logical 1 on line E is generated by the monostable multivibrator 19. "One-shot" devices such as monostable multivibrator 19 are well known in the art and available commercially, for example, the Fairchild product 9600. In one embodiment of this invention line T is connected to a location in the chain of frequency dividers $11c...11_k$. to receive therefrom a signal every 20 seconds. This signal every 20 seconds causes one-shot 19 to supply a signal on line E, thereby enabling NAND gates 21a, 21b, and 21c. The enabling of NAND gates 21a, 21b, and 21c allows the information presented at terminals I1, I2, and I4 to be loaded into programmable down counters 23a, 23b, and 23c.

The signals presented to terminals I1, I2 and I4 may be supplied in several different ways. For example, if it is desired to permanently program the circuit shown in Figure 2 to add or subtract a selected number of pulses at selected intervals determined by the frequency of the signal on line T

then selected ones of terminals I1, I2, and I4 may be "hard-wired" to a voltage supply. On the other hand, if the average frequency supplied on line OUT is to be changed periodically, such as would be the case if the frequency of signals supplied by frequency source 11 changes with time, then terminals I1, I2 and I4 may be selectively supplied with signals by some other electronic circuit or external switching means. In the electronic time keeping arts a switch on the exterior of a watch case could be used to supply signals to well-known logic-controlling terminals I1, I2, and I4.

An example will further clarify the function and operation of circuit 28. Assume that by utilizing testing equipment external to the digital watch it is discovered that the quartz crystal oscillator frequency is twelve parts per million lower than that required for perfect time. For a quartz crystal oscillator vibrating at a frequency of 100,000 hertz, this is equivalent to an error of 72 cycles of the fundamental oscillator frequency every minute. (In an embodiment of this invention in which the wearer of the digital watch may use a switch on the exterior of the case to supply signals to terminals I1, I2, and I4, similar information would be obtained by observing that the watch is about 30 seconds slow every month.) It is therefore desired to add 72 pulses every minute to the signal being supplied by frequency source 11.

This is accomplished utilizing the circuit shown in Figure 2 as follows. Assume counter 11a is a divide by two circuit and counter 11b is a divide by six circuit. During assembly of the digital watch, terminals I2 and I4 are connected to a voltage source, and terminal I1 is not so connected. Line T, which connects one-shot device 19 to the chain of dividers 11a, 11b, 11c...11k, is connected following a divider which provides a signal every one minute. Terminal I+, because it is desired to add pulses to the signal being supplied by frequency source 11, rather than subtract pulses, is also connected to a voltage source during assembly of the watch. Therefore, every one minute a signal will appear on line T to activate one-shot device 19. This will enable NAND gates 21b and 21c allowing the logical 1 to activate counters 23b and 23c, causing six pulses to be supplied on line G to NAND gate 35. In the manner previously explained the six pulses appearing on line G will result in six additional pulses appearing on line OUT. These six additional pulses will eventually be supplied to divider 11k, thereby in effect correcting the time indicated on the watch display. It should be noted however, that the magnitude of the correction, if it is less than one second, will not appear on the display and be visible to the user. For example, the addition of six pulses every minute will not be observed by the wearer of the watch, who would be unaware that every minute one second is slightly shorter in duration than all other seconds being displayed by the watch during the one minute period.

Counters 23a, 23b and 23c may be chosen from many types of commercially available counters, however, programmable down counters such as the Fairchild 340193 have been found suitable. Once signals from the NAND gates 21a, 21b and 21c are stored in counters 23a, 23b, and 23c, respectively, whenever any of the counters 23a, 23b, and 23c present a logical 1 to any of lines Q1, Q2, and Q3, OR gate 24 will cause a logical 1 to appear at terminal G, thereby enabling AND gate 29 to allow clock pulses on line V to begin to decrement counters 23a, 23b, and 23c. When any counter reaches zero a logical 0 will appear at the output from that counter. When all three counters have counted down to zero, OR gate 24 will cause a logical 0 to appear on line G. This logical 0 disables AND gate 29 and clock pulses on line V are no longer supplied to the counters 23a, 23b, and 23c. In this fashion counters 23a, 23b, and 23c control the duration of a given signal, either 1 or 0 on line G. In the embodiment shown in Figure 2 this duration t_G is given by the equation:

$$t = \frac{(1 \times I1 + 2 \times I2 + 4 \times I4)}{f_{in}}$$

where f_{in} is the frequency on line IN, and where I1, I2 and I4 equal 0 or 1. Thus, the number of pulses k which are added or subtracted during time t will be given by:

$$k + I1 + 2I2 + 4I4$$

Although only three input terminals I1, I2 and I4 and only three counters 23a, 23b and 23c are shown in Figure 2, it will be obvious to those skilled in the digital arts that any number of inputs I1, I2, I4...I_j can be used in conjunction with a corresponding number of counters 23a, 23b...23$_j$ and an expanded OR gate 24. Using Fairchild 340193 counters the number of pulses which may be added or subtracted by j inputs will be given by:

$$k = I1 + 2I2 + 4I4 + \ldots + mI_m$$

where $m = 2^{j-1}$.

A sample timing diagram for the logic diagram shown in Figure 2 appears as Figure 3. The location in the schematic of Figure 2 of the signals displayed in Figure 3 is shown down the left hand side of Figure 3. Figure 3a shows the clock pulses on line IN supplied by divider 11a to circuit 30. The signal on line E to enable the addition or subtraction pulses is shown as Figure 3b. A hypothetical logical 1 condition of terminal I1 and terminal I4, and a hypothetical logical 0 condition of terminal I2 are shown as Figures 3c, 3e, and 3d, respectively. The signals on terminals I1, I2, and I4 cause the counters 23a, 23b, and 23c to present output signals shown in Figure 3f, 3g, and 3h, respectively. These output signals result in a logical 1 at terminal G for the period depicted in Figure 3i. If the signal on line I+ is a logical 0 as shown in Figure 3j, then a subtract pulse condition exists and the output wave form is shown as the signal OUT_{sub} in Figure 3k. If, instead as shown in Figure 3m, terminal I+ is a logical 1 then an add

pulse condition exists and the output signal appears as signal OUT_{add} shown in Figure 3n.

CLAIMS

1. A circuit for adjusting the average frequency of signals supplied to its output means comprising:

a source of signals,

a frequency dividing means having an input and an output,

first switch means connected in series with the frequency dividing means between the source and the output means,

second switch means connected between the source of signals and the output means in parallel with at least the frequency dividing means, and

control means for selectively engaging and disengaging the first switch means and the second switch means.

2. A circuit as shown in claim 1 wherein the second switch means is connected in parallel with both the first switch means and the frequency dividing means.

3. A circuit as in claim 2 wherein:

the first switch means includes a first NAND gate and a second NAND gate,

the second switch means includes a third NAND gate and the second NAND gate, wherein a first input terminal of the first NAND gate is connected to the control means, and a second input terminal of the first NAND gate is connected to the output of the frequency dividing means, a first terminal of the third NAND gate is connected to the control means and a second terminal of the third NAND gate is connected to the input of the frequency dividing means, a first input terminal of the second NAND gate is connected to an output terminal of the first NAND gate and a second input terminal of the second NAND gate is connected to an output terminal of the third NAND gate, and

the output means of the circuit for adjusting the average frequency is an output terminal of the second NAND gate.

4. A circuit as in claim 3 wherein a plurality of input terminals to the control means receive information indicative of a desired state of the first and the second switch means.

5. A circuit as in claim 4 wherein the plurality of input terminals is four input terminals, and the first, second, and third input terminals are connected to receive information indicative of the amount of adjustment to the average frequency, and the fourth input terminal is connected to receive information indicative of whether the average frequency is to be increased or decreased.

6. A circuit as in claim 5 wherein:

the first input terminal to the control means is connected to a fourth NAND gate,

the second input terminal to the control means is connected to a fifth NAND gate,

the third input terminal to the control means is connected to a sixth NAND gate, and wherein each of the fourth, fifth, and sixth NAND gates is also connected to receive signals from a first source of signals of known relationship to the signals from the source of signals.

7. A circuit as in claim 6 wherein the control means includes at least one counter, the at least one counter being connected to a second source of signals of known relationship to the signals from the source of signals.

8. A circuit as in claim 7 wherein the first source of signals is a monostable multivibrator, and the second source of signals is the source of signals.

9. A circuit as in claim 7 wherein the at least one counter includes a first, a second and a third counter, and the fourth NAND gate is connected to the first counter, the fifth NAND gate is connected to the second counter, and the sixth NAND gate is connected to the third counter.

10. A circuit as in claim 9 wherein signals from at least one of the first, second, and third counters are supplied to at least one of the first input terminal of the first NAND gate and the first input terminal of the third NAND gate.

11. A circuit as in claim 1 wherein:

the source of signals includes a quartz crystal oscillator, and

the output means includes a series of counters to provide a count indicative of the time.

12. In an electronic time keeping apparatus, a circuit for adjusting the average frequency of signals supplied by a frequency source to a series of counters to provide a count indicative of the time comprising:

a frequency dividing means having an input and an output,

first switch means connected in series with the frequency dividing means between the source and the output means,

second switch means connected between the source of signals and the output means in parallel with at least the frequency dividing means, and

control means for selectively engaging and disengaging the first switch means and the second switch means.

13. A circuit for adjusting the average frequency of signals supplied to its output means substantially as herein described with reference to the accompanying drawings.

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